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APPL. NO.: 09-024566 [JP 9724566]
FILED: January 24, 1997 (19970124)
INTL CLASS: [6] H04J-013/00; H04B-007/26; H04L-007/00
JAPIO CLASS: 44.2 (COMMUNICATION -- Transmission Systems); 44.3 (COMMUNICATION -- Telegraphy)

ABSTRACT

PROBLEM TO BE SOLVED: To shorten the time of code synchronous detection of spectrum spread and to prevent the degradation of synchronous detection characteristics in a CDMA mobile communication system.
SOLUTION: On the transmission side, first, second,..., N-th spread codes are used for (a+1)th, (a+2)th,... (a+N)th symbols ((a) is an arbitrary integer) of information modulation symbols on the transmission side to perform spectrum spread and transmission. On the reception side, matched filters 22 to 24 matched to first,..., N-th spread codes are used to obtain a correlation waveform from a reception signal. A delay circuit 25 is used to delay this correlation waveform by 0 to N-1 information modulation symbols times, and the sequence of peak detection of correlation is detected to perform discrimination of a base station and detection of code synchronization. Thus, the time of code synchronous detection is shortened and the degradation of synchronous characteristics is prevented in comparison with the use of a sliding correlator.
?T 5436488/5

5436488/5

05436488 **Image available**
SPREAD SPECTRUM RECEIVING DEVICE

PUB. NO.: 09-051288 [JP 9051288 A]
PUBLISHED: February 18, 1997 (19970218)
INVENTOR(s): SUGAWARA YOJI
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APPL. NO.: 07-198351 [JP 95198351]
FILED: August 03, 1995 (19950803)
INTL CLASS: [6] H04B-001/707
JAPIO CLASS: 44.5 (COMMUNICATION -- Radio Broadcasting); 44.2 (COMMUNICATION -- Transmission Systems)

ABSTRACT

PROBLEM TO BE SOLVED: To reduce a synchronization acquisition time by varying the number of stages of matched filters corresponding to a reception state in the spread spectrum receiver used for mobile communication so as to enhance the general- purpose performance of the receiver.
SOLUTION: A synchronization detection circuit 24 of the spread spectrum receiver receives a correlation output from a matched filter 1 and a synchronization/asynchronization state signal fed from a delay locked loop DLL 5. When the synchronization detection circuit 24 detects an asynchronous state, the circuit 24 gives a correlation output to a threshold level generating circuit 22 and a 1-tip delay circuit 24, then the 1-tip delay circuit 23 gives the correlation output of one preceding tip to the threshold level generating circuit to receive a current correlation output. The threshold level generating circuit 22 compares the received correlation output with the correlation output of one preceding tip to decide the number of stages of SR for the matched filter. In the case of taking synchronization, a high correlation output is obtained

earlier depending on the small/high stage numbers to have provision for the change in a spread rate thereby enhancing the general-purpose performance.

?B351

09may02 10:00:10 User034901 Session D11729.2
Sub account: 027557-081
$2.54 0.232 DialUnits File347
$3.20 2 Type(s) in Format 5
$3.20 2 Types
$5.74 Estimated cost File347
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$5.95 Estimated cost this search
$6.28 Estimated total session cost 0.305 DialUnits

File 351:Derwent WPI 1963-2001/UD,UM &UP=200229
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***File 351: Please see HELP NEWS 351 for details about U.S. provisional** applications.

Set	Items	Description

?T 011604324/5

011604324/5
DIALOG(R)File 351:Derwent WPI
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011604324 **Image available**
WPI Acc No: 1998-021452/199803
XRPX Acc No: N98-016390

Communication system synchronisation method for high speed frequency hopping systems - using coincidences relative to threshold between detected and expected sequence in integration windows which have different durations

Patent Assignee: THOMSON CSF SA (CSFC); THOMSON CSF (CSFC)
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Number of Countries: 002 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
FR 2748876	A1	19971121	FR 889461	A	19880712	199803	B
IT 1275841	B	19971020	IT 8967524	A	19890628	199826	

Priority Applications (No Type Date): FR 889461 A 19880712
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
FR 2748876	A1		22	H04L-007/00	
IT 1275841	B			H04B-000/00	

Abstract (Basic): FR 2748876 A

The method involves integrating a call sequence using a number of windows of different durations. A first sliding frequency window is short and has a number of monitoring levels which give a coarse synchronisation when the sum of integrated values exceeds a first threshold. This sets off a verification phase on a fixed short duration window which looks for an integration sum passing a second threshold to determine synchronisation.

At the same time, another larger sliding frequency window comprising more levels is integrated to another threshold. The verification phase interrupts the integration and when the second threshold is not reached, the values leading to the passing of the first threshold are deleted before the first window slides.

ADVANTAGE - Synchronisation is entirely automatic, high speed and accurate.

Dwg.6/6

Title Terms: COMMUNICATE; SYSTEM; SYNCHRONISATION; METHOD; HIGH; SPEED;